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DAVID E. LOVEJOY, REG. NO. 22,748
102 REED RANCH ROAD
TIBURON, CA 94920-2025

EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 05/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,130	HILTON, RONALD	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-17 and 19-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-17 and 19-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/11/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-3, 5-17, 19-28 has/have been presented for examination based on amendment filed on 10th February 2006 and remarks filed on
2. Claim(s) 1, 5, 10, 11, 12, 15, 19, 24, 25 and 26 are amended.
3. Claim(s) 4 and 18 are cancelled.
4. The arguments submitted by the applicant have been fully considered. Claims 1-3, 5-17, 19-28 remain rejected. The examiner's response is as follows.

Response to Applicant's Remarks & Examiner's Withdrawals

5. Examiner withdraws the objection(s) to Oath in view of the new Oath filed on 30th December 2005.
6. Examiner withdraws the claim objection(s) to drawings in view of the amendment to Fig.1 and Fig.2.
7. Examiner withdraws the claim rejection(s) under 35 USC § 112 to claim(s) 1, 11, 15 and 25 in view of applicant's amendment and arguments.
8. Examiner maintains the claim interpretation, as TLB and indexing table being claimed are similar.
9. Examiner withdraws the claim rejection(s) under 35 USC § 101 to claim(s) 1-2, 4-10, 11-12, 15-16, 18-24 & 25-26 in view of applicant's amendment.
10. Examiner withdraws the claim rejection(s) under 35 USC § 102 to claim(s) 1-3, 7-9, 15-17 & 21-23 in view of applicant's amendments.

Response to Applicant's Remarks for 35 U.S.C. § 103

11. Claims 1-3, 5, 7-13, 15-17, 19, 21-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6516295 issued to George A. Mann et al (Mann '295 hereafter), further in view of ACM Article "Cache Memories" by Alan Jay Smith (Smith '1982 hereafter).

Regarding Claim 1

Applicant has argued that No one skilled in the art would believe that a simple indexing table is interchangeable with a TLB. Examiner agrees with the applicant, however the argument is not if an indexing table (of applicant) can perform the function of the TLB, but if the TLB (of the prior art) can be used as indexing table. In this case TLB can perform the function of the indexing table, therefore applicant's allegations are unpersuasive. MPEP 2131.02 states:

> "A generic claim cannot be allowed to an applicant if the prior art discloses a species falling within the claimed genus." The species in that case will anticipate the genus.

Further, applicant's arguments are not directed towards the claimed limitations. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., indexing table) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Although examiner agrees that TLB and indexing table "are not the same thing" and the TLB as agreed by the applicant is a more "complex structure", however it meets

the limitations recited in the claim. Applicant's arguments have been fully considered but they are not persuasive.

Further, in section 10.5 applicant argues that it is unclear how Mann'295 presents any problem that is solved by Smith'1982. Mann'295 teaches reuse of the translated code by multiple blocks (Mann'295: Col.6 Lines 62-Col.7 Line 3) which are chained together. The portion cited earlier is preceding paragraph citing the chaining mechanism. The reuse of the code by other block entry tables requires a many to one or one to many mapping between the translated code in the host code block and block entry tables. This deficiency is not addressed in Mann'295 and would be necessary for efficient code reuse (Problem to be solved). Smith'1982 teaching as described earlier in the rejection cures this deficiency. Hence the motivation to combine is well founded based on the implementation of the Mann'295 teachings.

Further, applicant argues, outside the claimed limitations, that the teachings of Mann'295 and Smith'1982 even if combined to not teach or suggest applicant's invention as Mann'295 teaches re-translation in every case, whereas applicant's invention avoids re-translation providing savings in execution time. This is not correct, Mann teaches translation until a certain number of times, kept as a count, and once the count is reached, stores the translation (DOCT) in the host code block for reuse (Fig.4 Element 122, 126 and Col.6 Lines 62-Col.7 Line 3) by other blocks. Further, Applicant's argue that such a combination (Mann'295 with Smith'1982) does not describe the avoidance of re-translation if instruction data has not been changed.

Examiner respectfully disagrees, as Mann'295 teaches this limitation (Mann'295: Col.7 Lines 4-37) where new Host code block is assigned for re-translation if the instructions are modified.

Applicants have not presented any new arguments regarding claims 6 & 20 (rejected with Mann'295 in view of Scalzi'013), claims 14 & 28 (rejected with Mann'295 in view of Smith'1982, further in view of Scalzi'013) and claims 8 & 22 (rejected with Mann'295 in view of applicant's own admission). These claims remain rejected based on the response presented above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 1-3, 5, 7-13, 15-17, 19, 21-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6516295 issued to George A. Mann et al (Mann '295 hereafter), further in view of ACM Article "Cache Memories" by Alan Jay Smith (Smith '1982 hereafter).

Regarding Claim 1

Mann '295 teaches a *computer-implemented* method of emulating execution of a legacy instruction (Mann '295: Col.2 Lines 44-51). Mann '295 teaches instructions having instruction address (Mann '295: Col.5 Lines 28-29).

Further, **Mann '295** teaches accessing blocks of legacy instruction (Mann '295: Col.6 Lines 11-12). **Mann '295** teaches blocks having block addresses (Mann '295: Col.6 Lines 17-19).

Further, **Mann '295** teaches storing *translations* into translation store as the host code block (Mann '295: Fig. 3 Element 88; Col.5 Lines 58-63; Col.6 Lines 11-28) for each legacy instruction.

Further, **Mann '295** teaches storing translation indication at block numbers determined by block addresses (Mann '295: Fig. 3 Element 81). Mann '295 teaches indexing table as block entry table for indicating that the block has been translated (Mann '295: Col.6 Lines 62-66).

Mann '295 teaches executing translated instructions to emulate the legacy instruction (Mann '295: Fig.4 Element 124).

Further, **Mann '295** teaches each particular legacy instruction of the translated block having a particular block number (Mann '295: Fig. 3 Element 72F-L, 80-81).

Further, **Mann '295** teaches translating a particular legacy instruction into one or more translated instructions for emulating the particular legacy instruction (Mann '295: Col.6 Lines 53-55).

Further, **Mann '295** teaches if a legacy instruction is not a store instruction, going to step of executing translated instruction as performing the DOCT (Mann '295: Col.9 Lines 5-10; Fig. 4 Elements: 126, 124, Fig. 5 Element 134/136 & 148).

Mann '295 teaches if the instruction is a store instruction, where the store instruction stores to a particular legacy block with a particular block number in the (block translation) table (Mann '295: Fig.4; Col.9 Lines 10-36, Col.7 Line 49-Col.8 Line 65).

Mann '295 teaches if the indication indicates that said particular block (of legacy instruction) has not been translated (indicated as X – do not translate), going to the step of executing the translated instruction (Mann '295: Fig.4 Path 108, 128, 129).

Mann '295 teaches checking if the instruction has been translated (Mann '295: Table T1, Non-X statuses; Fig.4), checking translation store to determine if the legacy instruction data has been modified, repeating the translation of legacy instruction (in new host code block starting with code 'F') then executing the instruction (Mann '295: Col.7 Lines 4-38; Fig.4; Col.9 Lines 9 –20). If the instruction data has not been modified then executing the translated instructions (Mann '295: Fig.4 Path 102, 110, 120, 124).

***On a closer review*, Mann'295 also teaches using index/offset (partial addresses) from the instructions as index for the block entry table, thereby teaching the limitation of "said storing translation indications using a subset**

of block address digits whereby block numbers in said table are the same for multiple different blocks" (Mann'295: Col. 6 Lines 16-24).

Mann'295 does not teach the details of the limitation presented above explicitly. Smith '1982 teaches that TLB having a hashing mechanism to map the virtual addresses (block numbers) to the real address (translated host code block) (Smith '1982: Pg.475 Col.2 Paragraphs 3-4). Hashing (done by taking an XOR or through randomized algorithm) depends on the number of bits selected, resulting in folding or overlapping (Smith '1982: Pg.488, Col.1 Paragraph 1; Pg.489, Col.1). The hashing scheme selected by the applicant is extremely simplified version, as only one middle bit is selected to index the translation indication index table.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to combine the teachings of Smith '1982 and apply them to Mann '295 to implement the indexing table as disclosed. The motivation would have been that Smith '1982 discloses the necessity for TLB like lookup when dealing with translated information when address space doesn't map directly (Smith '1982: Pg.510, Section 2.9, 2.17). Mann '295's design requires translation as one target code block may have one or more translated host code instructions. Hence Smith '1982 solves Mann '295's problem of mapping the target legacy instruction object to translated host object code block (Mann '295: Col.6 Lines 47-55). Please see further the response to arguments for clarification.

Regarding Claim 2

Mann '295 teaches the step of storing translation indications for only a subset of all translated blocks (Mann '295: Col.5 Lines 54-63).

Regarding Claim 3

Mann '295 storing the translated executable host code on the volatile cache memory like SRAM (Mann '295: Col.3 Lines 36-38, 55-61; Col.4 Lines 16-18).

Regarding Claim 5

From the teachings of Mann'295 and Smith'1982 it obvious to use the subset (middle 3 hexadecimal) of digits form the legacy instruction for the part of the address field of the indexing table (Mann'295: Col. 6 Lines 16-24; Smith'1982: Pg.475 Col.2 Paragraphs 3-4; Pg.488, Col.1 Paragraph 1; Pg.489, Col.1).

Regarding Claim 7

Mann '295 teaches that legacy instructions are object code instructions compiled/assembled for the legacy architecture (Mann '295: Col.2 Lines 44-51).

Regarding Claim 8

Mann '295 teaches legacy instruction includes store instructions for modifying instruction code (Mann '295: Col.9 Lines 5-20, 38-47; Col.7 Lines 14-37).

Regarding Claim 9

Mann '295 teaches translation indication includes a state field as tag field, for each block number, indicating the block has been modified (Mann '295: Col.5 Table 1; Col.6 Lines 62-67).

Regarding Claim 10

Mann '295 teaches storing the translated executable host code on the volatile cache memory like SRAM (Mann '295: Col.3 Lines 36-38, 55-61; Col.4 Lines 16-18).

Further, Mann '295 teaches that the translation indication includes a state field (tag field), for each block number, indicating the block has been modified (Mann '295: Col.5 Table 1; Col.6 Lines 62-67). Further, Mann '295 teaches incrementing the state field each time block is executed on the cache (Mann '295: Col.6 Lines 64-65).

It would have been obvious to keep track of modification to the block as modifications are already kept track at each legacy instruction level (Mann '295: Col.7 Lines 13-38). Mann '295 does not teaches decrementing the count, but teaches equivalent functionality of removing and de-allocating the block entry table (indexing table entry) when the translated host block is no longer needed/garbage collected (Mann '295: Col.7 Lines 62-67, Col.8 Lines 1-3). Further, Mann '295 teaches bypassing the checking if there is no store instruction data (Mann '295: Fig. 5 Element 134/136 & 148).

Regarding Claim 11

Mann '295 teaches a method of dynamic emulating execution of a legacy instruction (Mann '295: Col.2 Lines 44-51). Mann '295 teaches instructions having instruction address (Mann '295: Col.5 Lines 28-29). Further, **Mann '295** teaches accessing blocks of legacy instruction (Mann '295: Col.6 Lines 11-12). **Mann '295** teaches blocks having block addresses (Mann '295: Col.6 Lines 17-19). Further, **Mann '295**

teaches storing *translations* into translated code into host code block (translation store) for each legacy instruction (Mann '295: Fig. 3 Element 88; Col.5 Lines 58-63; Col.6 Lines 11-28).

Further, **Mann '295** teaches storing translation indication at block numbers determined by block addresses (Mann '295: Fig. 3 Element 81). Mann '295 teaches indexing table as block entry table for indicating that the block has been translated (Mann '295: Col.6 Lines 62-66).

Mann '295 teaches executing translated instructions to emulate the legacy instruction (Mann '295: Fig.4 Element 124).

Further, **Mann '295** teaches each particular legacy instruction of the translated block having a particular block number (Mann '295: Fig. 3 Element 72F-L, 80-81).

Further, **Mann '295** teaches translating a particular legacy instruction into one or more translated instructions for emulating the particular legacy instruction (Mann '295: Col.6 Lines 53-55).

Further, Mann '295 teaches checking store instruction associated to the block entry table, if instruction data is stored (Mann '295: Col.9 Lines 5-10; Fig. 4 Elements: 126, 124, Fig. 5 Element 134/136 & 148) for a particular block. Mann '295 also teaches checking if the instruction data has been modified (Mann '295: Col.9 Lines 9 –20).

Further, Mann '295 teaches bypassing the checking if there is no store instruction data (Mann '295: Fig. 5 Element 134/136 & 148). Further, **Mann '295** teaches the step of storing translation indications for only a subset of all translated blocks (Mann '295: Col.5 Lines 54-63).

Mann '295 teaches if the instruction is a store instruction, where the store instruction stores to a particular legacy block with a particular block number in the (block translation) table (Mann '295: Fig.4; Col.9 Lines 10-36, Col.7 Line 49-Col.8 Line 65).

Mann '295 teaches if the indication indicates that said particular block (of legacy instruction) has not been translated (indicated as X – do not translate), going to the step of executing the translated instruction (Mann '295: Fig.4 Path 108, 128, 129).

Mann '295 teaches checking if the instruction has been translated (Mann '295: Table T1, Non-X statuses; Fig.4), checking translation store to determine if the legacy instruction data has been modified, repeating the translation of legacy instruction (in new host code block starting with code 'F') then executing the instruction (Mann '295: Col.7 Lines 4-38; Fig.4; Col.9 Lines 9 –20). If the instruction data has not been modified then executing the translated instructions (Mann '295: Fig.4 Path 102, 110, 120, 124).

Mann '295 teaches storing the translated executable host code on the volatile cache memory like SRAM (Mann '295: Col.3 Lines 36-38, 55-61; Col.4 Lines 16-18).

Mann '295 teaches translation indication includes a state field as tag field for each block number indicating the block has been modified (Mann '295: Col.5 Table 1; Col.6 Lines 62-67).

Regarding Claim 12

Method claim 12 is directed towards similar limitations as the method claim 10 and is rejected for the same reason as claim 10.

Regarding Claim 13

Mann '295 teaches that legacy instructions are object code instructions compiled/assembled for the native legacy architecture executed as guest on host architecture (Mann '295: Col.2 Lines 44-51, Fig.3).

Regarding Claim 15

Mann '295 teaches an apparatus and a method for emulating self-modifying code. The system claim 15 is directed towards the same limitations as the method claim 1 and is rejected for the same reason as claim 1.

Regarding Claim 16

The system claim 16 is directed towards the same limitations as the method claim 2 and is rejected for the same reason as claim 2.

Regarding Claim 17

The system claim 17 is directed towards the same limitations as the method claim 3 and is rejected for the same reason as claim 3.

Regarding Claim 19

The system claim 19 is directed towards the same limitations as the method claim 5 and is rejected for the same reason as claim 5.

Regarding Claim 21

The system claim 21 is directed towards the same limitations as the method claim 7 and is rejected for the same reason as claim 7.

Regarding Claim 22

The system claim 22 is directed towards the same limitations as the method claim 8 and is rejected for the same reason as claim 8.

Regarding Claim 23

The system claim 23 is directed towards the same limitations as the method claim 9 and is rejected for the same reason as claim 9.

Regarding Claim 24

The system claim 24 is directed towards the same limitations as the method claim 10 and is rejected for the same reason as claim 10.

Regarding Claim 25

The system claim 25 is directed towards the same limitations as the method claim 11 and is rejected for the same reason as claim 11. Further, Mann '295 storing the translated executable host code on the volatile cache memory like SRAM (Mann '295: Col.3 Lines 36-38, 55-61; Col.4 Lines 16-18).

Regarding Claim 26

The system claim 26 is directed towards the same limitations as the method claim 10 and is rejected for the same reason as claim 10.

Regarding Claim 27

The system claim 27 is directed towards the same limitations as the method claim 13 and is rejected for the same reason as claim 13.

13. Claims 6 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,516,295 issued to George A. Mann et al (Mann '295 hereafter) in view of U.S. Patent No. 5,560,013 issued to Casper A. Scalzi et al (Scalzi '013 hereafter).

Regarding Claim 6

Teachings of Mann '295 are disclosed in the claim 1 rejection above.

Mann '295 does not teach legacy instructions are for a legacy system having S/390 Architecture.

Scalzi '013 teaches that legacy instructions are for a legacy system having S/390 Architecture (Scalzi '013: Col.17 Lines 54-57).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to combine the teachings of Scalzi '013 and apply them to Mann '295 to emulate execution of legacy instruction for S/390 legacy architecture. The motivation would have been that Scalzi '013 and Mann '295 are analogous art and Scalzi '013 is performing the instruction set translation in a very similar fashion as Mann '295 through mapping/dynamic address translation (Scalzi '013: Col. 5 Lines 17-23) and instruction-self-modification (Scalzi '013: Col.12 Lines11-24; Col.14 Lines 16-24).

Regarding Claim 20

The system claim 20 is directed towards the same limitations as the method claim 6 and is rejected for the same reason as claim 6.

14. Claims 14 & 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,516,295 issued to George A. Mann et al (Mann '295 hereafter) in view of ACM Article "Cache Memories" by Alan Jay Smith (Smith '1982 hereafter), further in view of U.S. Patent No. 5,560,013 issued to Casper A. Scalzi et al (Scalzi '013 hereafter).

Regarding Claim 14

Teachings of Mann '295 & Smith '1982 are disclosed in the claim 11 rejection above.

Mann '295 & Smith '1982 do not teach emulated execution by translation from CISC based legacy instruction set to the RISC based target/host instruction set.

Scalzi '013 teaches that legacy instructions are for a legacy system having S/390 Architecture which is a CISC architecture and host architecture is power PC (RISC) based architecture (Scalzi '013: Col.17 Lines 54-57).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to combine the teachings of Scalzi '013 and apply them to Mann '295 to emulate execution of legacy instruction for S/390 legacy architecture. The motivation would have been that Scalzi '013 and Mann '295 are analogous art and Scalzi '013 is performing the instruction set translation in a very similar fashion as Mann '295 through mapping/dynamic address translation (Scalzi '013: Col. 5 Lines 17-23) and instruction-self-modification (Scalzi '013: Col.12 Lines11-24; Col.14 Lines 16-24).

Regarding Claim 28

Teachings of Mann '295 & Smith '1982 are disclosed in the claim 25 rejection above. The system claim 28 is directed towards the same limitations as the method claim 14 and is rejected for the same reason as claim 14. To facilitate prosecution rejection is repeated below.

Mann '295 & Smith '1982 do not teach emulated execution by translation from CISC based legacy instruction set to the RISC based target/host instruction set.

Scalzi '013 teaches that legacy instructions are for a legacy system having S/390 Architecture which is a CISC architecture and host architecture is power PC, RISC based architecture (Scalzi '013: Col.17 Lines 54-57).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to combine the teachings of Scalzi '013 and apply them to Mann '295 to emulate execution of legacy instruction for S/390 legacy architecture. The motivation would have been that Scalzi '013 and Mann '295 are analogous art and Scalzi '013 is performing the instruction set translation in a very similar fashion as Mann '295 through mapping/dynamic address translation (Scalzi '013: Col. 5 Lines 17-23) and instruction-self-modification (Scalzi '013: Col.12 Lines11-24; Col.14 Lines 16-24).

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Akash Saxena
Patent Examiner, GAU 2128
(571) 272-8351
Friday, May 12, 2006

Fred Ferris
Primary Examiner, GAU 2128
Structural Design, Modeling, Simulation and Emulation
(571) 272-3778